



DPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKIMOTO, Kyuichi, et al.**

Group Art Unit: **2838**

Serial No.: **10/624,644**

Examiner: **Gary L. LAXTON**

Filed: **July 23, 2003**

P.T.O. Confirmation No.: **6904**

For: **CONTROL CIRCUIT FOR DC/DC CONVERTER**

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 25, 2005

Sir:

In response to the Office Action dated **May 26, 2005**, Applicants respectfully request reconsideration of the following prior art rejections discussed below:

(1) The 35 U.S.C. § 102(b) rejection of claims 1, 2, 7, 14, 15 and 21 as anticipated of U.S. Patent 5,627,460 to Bazinet et al. (hereafter "Bazinet et al.").

Bazinet et al. discloses a synchronous step-down DC to DC converter including a bootstrap capacitor monitored by a controller for maintaining a desired bootstrap voltage to drive a high side NMOS switch. The controller temporarily increases the duty cycle of the low side NMOS switch when the bootstrap voltage decreases below a predetermined level to maintain a minimum level of charge on the bootstrap capacitor.

As shown in FIG. 6, Bazinet et al. discloses providing the NOR circuit 178, which generates a gate drive signal 40 of the switch 14, with a gate drive signal 38 for driving the switch 12 and providing the NOR circuit 176, which generates the gate drive signal 38, with the

gate drive signal 40. In this case, because there is a delay when the gate drive signals pass through the NOR circuits 176, 178 and the gate drive signals are affected by gate capacitance of the switches 12 and 14, the gate drive signal 28 cannot have the same pulse width as that of the PWM command signal 62. In FIG. 3 of Bazinet et al., although it appears that the gate drive signal 38 has the same pulse width as that of the PWM command signal 62, they are actually not the same. Furthermore, because the gate drive signals 40 and 38 rise and fall at the same time, they are turned ON simultaneously, thereby flowing through current.

Thus, Bazinet et al. does not disclose the drive signal generation circuit that generates first and second drive signals such that a main switching element and a synchronous switching element are turned ON and OFF alternately at different timings and the first drive signal has the same pulse width as that of a pulse signal, as recited in each of claims 1, 7, 14 and 21.

Thus, the 35 U.S.C. § 102(b) rejection of claims 1, 2, 7, 14, 15 and 21 should be reconsidered and withdrawn.

(2) The 35 U.S.C. § 103(a) rejection of claims 3, 8-10, 16 and 20 as unpatentable over Bazinet et al. in view of Nishimaki (previously applied).

Neither Nishimaki nor Bazinet et al. disclose the drive signal generation circuit of the present invention. As shown in FIG. 8, Nishimaki discloses providing the NAND gate 322, which generates a pulse signal SL of the NMOS transistor QN1, with a pulse signal SH for driving the PMOS transistor QP1 and providing the NAND gate 321, which generates the pulse signal SL, with the pulse signal SH. In this case, since there is a delay when the pulse signals

pass through the NAND circuits 321, 322 and the pulse signals are affected by gate capacitance of the transistors QP1 and QN1, the pulse signal SH cannot have the same pulse width as that of the PWM signal.

Thus, Nishimaki cannot be combined with Bazinet et al. to teach the present invention, and the 35 U.S.C. § 103(a) rejection of claims 3, 8-10, 16 and 20 should be reconsidered and withdrawn.

(3) The 35 U.S.C. § 103(a) rejection of claims 4, 11 and 17 as unpatentable over Bazinet et al. and Nishimaki in view of Bridge (previously applied).

None of Bazinet et al., Nishimaki or Bridge disclose the drive signal generation circuit of the present invention. As shown in FIG. 18b, Bridge generates a signal G1 having a pulse width that is smaller than that of the input signal IN.

Thus, the 35 U.S.C. § 103(a) rejection of claims 4, 11 and 17 should be reconsidered and withdrawn.

(4) The 35 U.S.C. § 103(a) rejection of claims 5, 12 and 18 as unpatentable over Bazinet et al. and Nishimaki in view of U.S. Patent 4,862,364 to Matsuda (hereafter “Matsuda”).

None of Bazinet et al., Nishimaki or Matsuda disclose the drive signal generation circuit of the present invention. Matsuda discloses the reset signal generator 26 that delays a reset signal using the delay circuit 28 comprising a resistor R10 and a capacitor C10.

Thus, the 35 U.S.C. § 103(a) rejection of claims 5, 12 and 18 should be reconsidered and withdrawn.

(5) The 35 U.S.C. § 103(a) rejection of claims 6, 13 and 19 as unpatentable over Bazinet et al. and Nishimaki in view of U.S. Patent 6,577,517 to Jain et al. (hereafter “Jain et al.”). Jain et al. discloses a pulse width modulation control circuit for a high frequency series resonant AC/DC converter suitable for use in computing and network equipment such as personal computers, servers and high-speed routers that includes an auxiliary transformer, a zero crossing detector, a delay circuit, a synchronization circuit and an output circuit. The Examiner has specifically cited Jain et al. for teaching a synthesis circuit including a NOR circuit.

Jain et al., like the other cited references, fails to teach, mention or suggest the limitations of claims 1, 10 and 16, from which claims 6, 13 and 19 respectively depend.

Thus, the 35 U.S.C. § 103(a) rejection of claims 6, 13 and 19 should be reconsidered and withdrawn.

In view of the aforementioned remarks, claims 1-21 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants’ undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

U.S. Patent Application Serial No. 10/624,644
Response to Office Action dated May 26, 2005

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

Wes Brooks
William L. Brooks
Attorney for Applicant
Reg. No. 34,129

WLB/ak
Atty. Docket No. 030879
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



23850

PATENT TRADEMARK OFFICE

Q:\HOME\AKERR\WLB\03\030879\response aug 2005